CLAIMS

1. A sense amplifier system for sensing the charge of a passive addressable charge-storing means (601), the system being characterized in comprising a pair of a first and second charge reference means (600a, 600b) connected in parallel and similar to the charge-storing means (601), said first charge reference means (600a) having the opposite polarization of the second charge reference means (600b), said first and second charge reference means (600a, 600b) and the charge storing means (601) having a common input node (AWL); first and second pseudo-differential reference sense amplifiers (RSA_1; RSA_2) being respectively connected with an output node (RBL_1; RBL_2) of one of the charge reference means, said first and second pseudo-differential amplifiers (RSA_1; RSA_2) being adapted for generating output reference signals to a common reference node (CHREF); and a pseudo-differential sense amplifier (SA) having a first input connected with the common reference node (CHREF) for receiving a common reference input signal and a second input for receiving an output signal from the charge-storing means (601); whereby the pseudo-differential sense amplifier (SA) is enabled to perform a threshold comparison and generating an output sense signal indicative of a polarization state of the charge-storing means.

2. A sense amplifier system according to claim 1, characterized by both the pseudo-differential reference sense amplifiers (RSA_1; RSA_2) and the pseudo-differential sense amplifier (SA) being identical pseudo-differential sense amplifier circuits.

3. A sense amplifier system according to claim 2, characterized in that each pseudo-differential sense amplifier (RSA_1; RSA_2) circuit comprises input differential pair transistors (402, 404) connected with a pair of cascoded transistors (410, 412), and current source biasing pair transistors cascoded (438, 440) with a pair of transistors (434, 436), said cascoding in each case increasing sense amplifier open-loop gain.

4. A sense amplifier system according to claim 3, characterized in the input transistors (402, 404) being p-channel transistors and the current source transistors n-channel transistors (438, 440), or vice versa.

5. A sense amplifier system according to claim 2, characterized in that each pseudo-differential sense amplifier circuit (RSA,

SA) comprises a semi-balanced dual input (IN, IND) with a balanced dual output (OUTM, OUTP).

6. A sense amplifier system according to claim 2, characterized in that each pseudo-differential sense amplifier circuit (SA) comprises a switched capacitor common feed-back loop (426, 428, 430, 432, 434, 436, 438, 440) to control output common mode voltage.

7. A sense amplifier system according to claim 2, characterized in that each pseudo-differential sense amplifier circuit (SA) comprises means (430, 432) for integral switched capacitor common mode self-bias generation.

8. A sense amplifier system according to claim 2, characterized in that each pseudo-differential sense amplifier circuit (SA) comprises an integral positive feed-back latch (420, 422).

9. A sense amplifier system according to claim 2, characterized in that each pseudo-differential sense amplifier circuit (SA) comprises means for auto-zero offset cancellation.

10. A sense amplifier system for sensing the charges of a plurality of passive addressable charge-storing means (701), characterized in comprising at least two pairs of a first and a second charge reference means (700) similar to the charge-storing means (701), said first charge reference means($700_{-,1}$) having the opposite polarization of the second charge reference means ($700_{-,2}$); each of said at least two pairs of charge reference means having a common input node (WL) and a pair of common output nodes (RBL_1, RBL_2) respectively connected with said first and said second charge reference means (700) in each of said at least two pairs thereof, each common input node (WL) of said at least two pairs of charge reference means (700) moreover being connected with at least two charge-storing means (701); first and second pseudo-differential reference sense amplifiers (RSA_1; RSA_2) being respectively connected with the first common output node (RBL_1) and the second common output node (RBL_2) of the charge reference means (700), said first and second pseudo-differential reference sense amplifiers (RSA_1; RSA_2) being adapted for generating output reference signals to a common reference node (CHREF); and at least two pseudo-differential sense amplifiers (SA), each having a first input (INP)

connected with said common reference node (CHREF) for receiving a common reference input signal and a second input (IN) respectively being connected with a common output node (BL) of respective one of said at least two charge storing means (701) for receiving respective output signals therefrom, said at least two charge-storing means (701) forming the elements of an orthogonal row and column array thereof and with each of the charge-storing means of a row being connected to one of said at least two common input nodes (WL) and each of the charge storing means of a column being connected to a common output node (BL); whereby each pseudo-differential sense amplifier (SA) is enabled to perform a threshold comparison and generating an output sense signal indicative of a polarization state of a selected charge-storing means (700) connected therewith.

11. A sense amplifier system according to claim 10, characterized in the common input nodes (WL) forming a portion of the word-line electrodes (WL) of a matrix-addressable array of charge-storing memory cells (700), the common output nodes (RBL) of the charge reference means (703) forming a pair of reference bit-line electrodes (RBL_1, RBL_2) the common output nodes (BL) of the charge storing means forming bit-line electrodes of said matrix-addressable array; each of the reference bit-line electrodes (RBL_1, RBL_2) being assigned to the first and second pseudo-differential reference sense amplifiers (RSA_1; RSA_2) respectively; and each of the other bit-line electrodes (BL) being assigned to one of the pseudo-differential sense amplifiers (SA), whereby in a readout cycle a polarization state of respective selected charge-storing memory cells (701) can be detected either sequentially or in parallel and compared with a reference value.

12. A sense amplifier system according to claim 11, characterized in the sense amplifier system being provided as a subblock (SB) in a block of more than one sense amplifier system of this kind, such that the sense amplifiers (RSA, SA) of a subblock are assigned to a corresponding number of bit-line electrodes (BL) in the matrix-addressable array; and the pair of reference bit lines (P/RBL) of respective subblocks (SB) being distributed among the bit lines (BL) of array.

13. A sense amplifier system according to claim 11, characterized in that the sense amplifier system comprises a multiplexer

(MUX) connected with the bit line electrodes (BL) of the matrix-addressable array; a number *k* of consecutive bit lines (BL) in the array defining a segment of all word-line electrodes therein (WL), said number *k* of segment-defining bit lines corresponding to the number of pseudo-differential sense amplifiers (SA) in the sense amplifier system; and a pair of reference bit line electrodes (P/RBL) being provided adjacent to the bit line electrodes (BL) in each word line segment and connecting pairs of reference charge storing means (700) in each word line segment; whereby the charge-storing memory cells (701) on a single word line electrode (WL) of a word line segment may be read in parallel, and all word line segments similarly in turn by applying an appropriate addressing protocol and multiplexing the bit-line electrodes (BL) of a selected word line segment to establish their parallel connection to respective pseudo-differential sense amplifiers of the sense amplifier (SA) system as provided.

14. A non-volatile passive matrix-addressable memory device comprising an electrically polarizable dielectric memory material exhibiting hysteresis, particularly a ferroelectric or electret material, wherein said memory material is provided in a layer contacting a first set and second set of respective parallel addressing electrodes (WL;BL), wherein the electrodes (WL) of the first set constitute word lines of the memory device and are provided in substantially orthogonal relationship to the electrodes (BL) of the second set, the latter constituting bit lines of the memory device, wherein memory cells (801) with a capacitor-like structure are defined in the memory material at the crossings between word lines and bit lines, wherein each memory cell can be selectively addressed for a write/read operation via a word line (WL) and bit line (BL), wherein a write operation to a memory cell (801) takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line and bit line defining the cell, wherein said applied voltage either establishes a determined polarization state in the memory cell (801) or is able to switch between the polarization states thereof, and wherein a read operation takes place by applying a voltage to the memory cell (801) and detecting at least one electrical parameter of an output current on the bit lines (BL), wherein a sense amplifier system according to claim 11 is provided for sensing said polarization states of said memory cells (801) during a read operation, and wherein said memory device is

characterized in that said sense amplifier system is a pseudo-differential

sense amplifier system comprising at least one system subblock (SB), and that said at least one system subblock (SB) comprises at least one pseudo-differential sense amplifier circuit (SA) for sensing a polarization state of at least one memory cell (801) during said read operation and at least one pseudo-differential reference sense amplifier circuit (RSA) for sensing a polarization state of at least one reference memory cell (800) during said read operation, said at least one former circuit (SA) being connected with said at least latter circuit (RSA) via a common node (CHREF).

15. A memory device according to claim 14, characterized in that said at least one system subblock (SB) comprises a plurality of said pseudo-differential sense amplifier circuits (SA) for sensing respective polarization states of a corresponding plurality of memory cells (801) during said read operation.

16. A memory device according to claim 14 or claim 15, characterized in that said at least one system subblock (SB) comprises two reference sense amplifier circuits (RSA_1, RSA_2) for sensing two reference memory cells (800) during said read operation, said reference ferroelectric memory cells (800) having opposite polarization states.

17. A memory device according to claim 16, characterized in that the first and the second reference sense amplifier circuits (RSA_1, RSA_2) are adapted for generating an average of a first and a second reference memory cell output signal to said common node (CHREF), and that said at least one sense amplifier circuit (SA) connected therewith is adapted for comparing the output signal at said common node (CHREF) with the output signal from a memory cell (801).

18. A memory device according to claim 14, characterized in that said at least one sense amplifier circuit (SA) and said at least one reference sense amplifier circuit (RSA) are realized with identical amplifier circuitry.

19. A memory device according to claim 18, characterized in that said identical amplifier circuitry (SA, RSA) comprises a reference side and an array side, said reference side mirroring the circuit structure of said array side.

20. A memory device according to claim 14,
characterized in that said pseudo-differential sense amplifier system comprises a plurality of system subblocks (SB).

21. A memory device according to claim 20,
characterized in that each subblock (SB) comprises a plurality of said sense amplifier circuits (SA) for sensing the polarization state of a corresponding number of memory cells.